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Si-Ge and Strain Si Technology

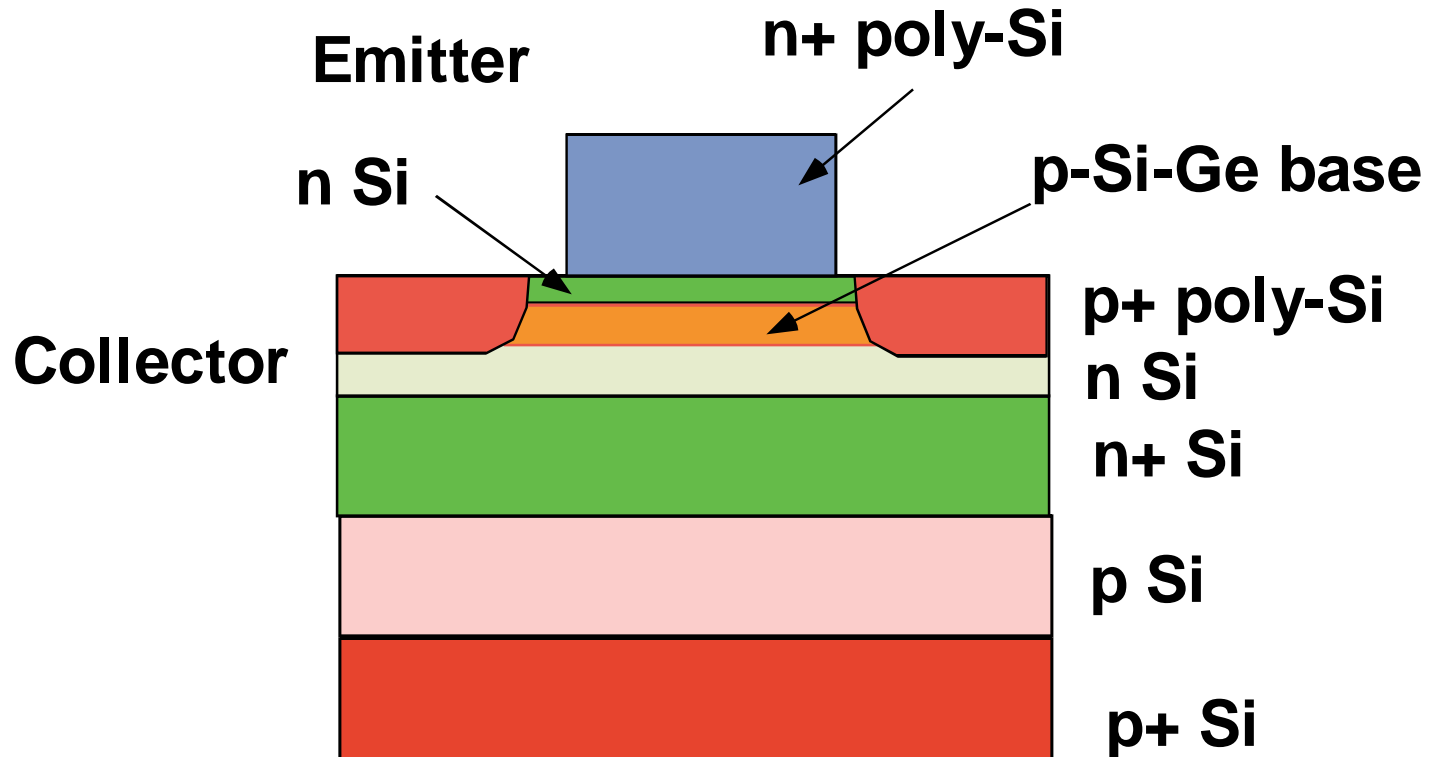
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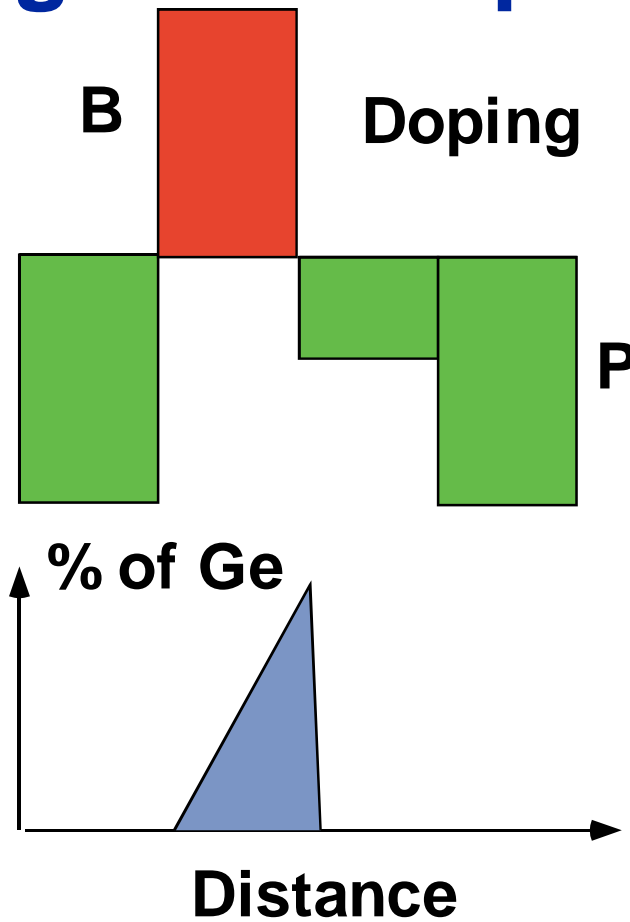
- Started in 1987 (IBM)
- Companies involved
 - IBM (US)
 - Analog Devices (US)
 - NEC (Japan)
 - Daimler Benz (Germany)
 - Nortel (Canada)
- Devices researched
 - HBT
 - HCMOS (CMOS)
 - Si-Ge optoelectronic

Si-Ge Technology in a Nutshell

Si-Ge Heterojunction Bipolar Transistor



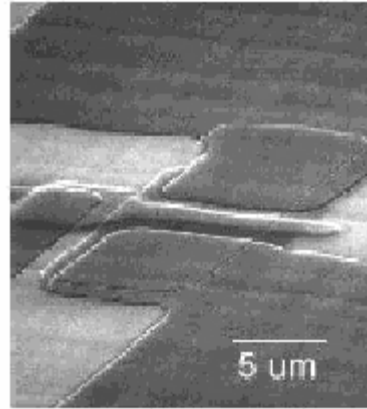
Doping and composition



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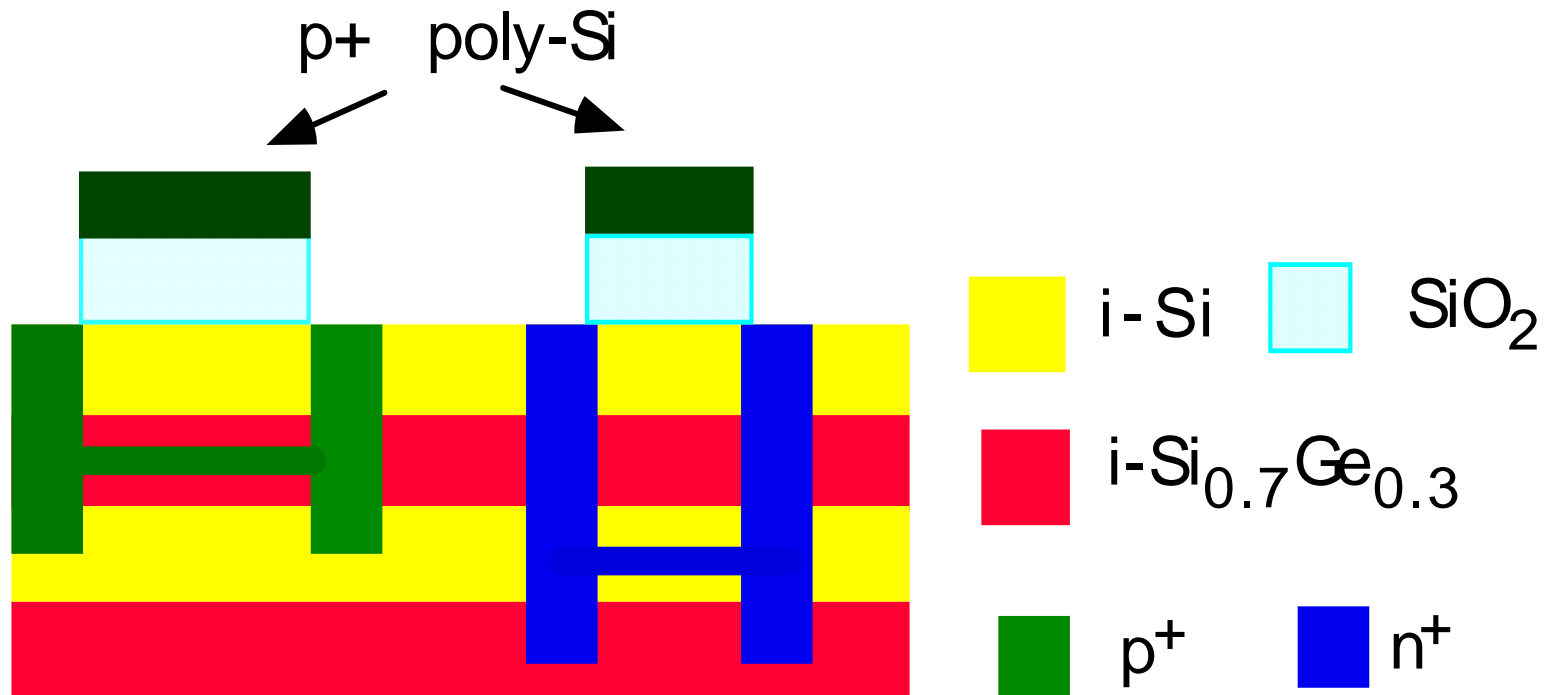
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**Si-Ge MOSFET
fabricated by Prof. Thomas Jackson Group
at Penn State**



See <http://jerg.ee.psu.edu/Research/Silicon-germanium/SiGe-MOSFET/>

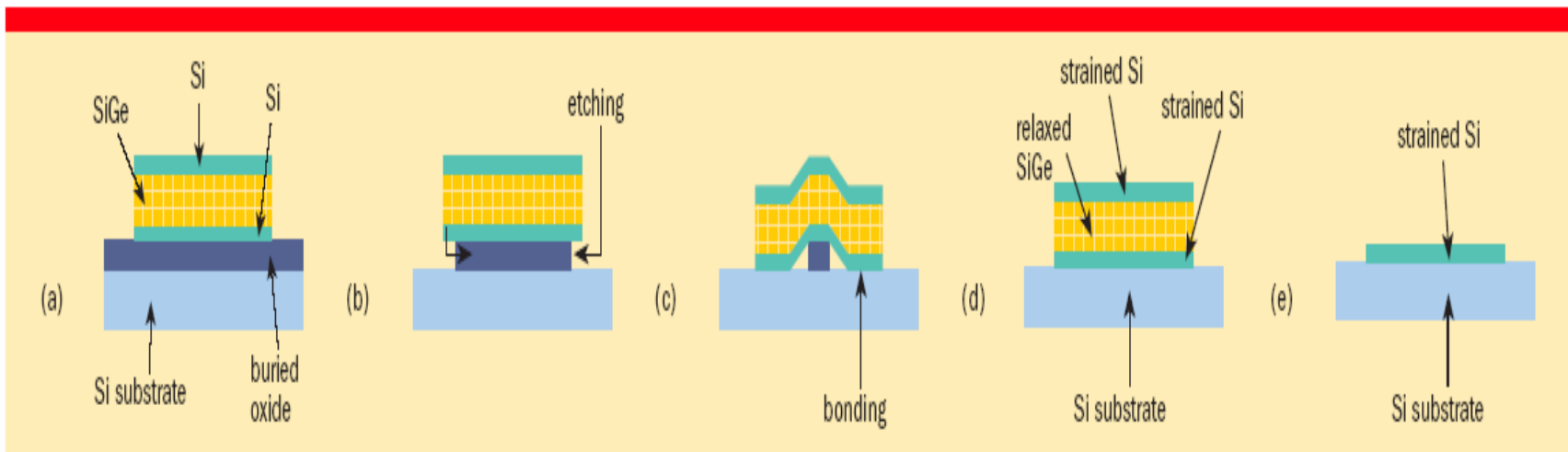
Si-Ge CMOS



Applications (expected)

- Wireless
- 2-30 GHz range
- Competition to GaAs
- replacement for Si BJT and GaAs-based HBTs

Smooth Strain Si from IBM



Fabrication of strained silicon-on-silicon structures begins with epitaxial growth of sequential silicon – $\text{Si}_{0.8}\text{Ge}_{0.2}$ – and silicon layers onto silicon-on-insulator substrates incorporating a 145 nm-thick layer of buried oxide. Reactive ion etching and conventional lithography then define isolated slabs in these epiwafers (a). This is followed by removing the buried oxide layer by etching with diluted hydrofluoric acid (b), which allows the SiGe layer to relax elastically and induce tensile strain in the silicon films (c). The free-standing silicon surface is then bonded to the silicon substrate by hydrophobic attraction (d). Adhesion between the two surfaces is strengthened by annealing for 3 h at 800 °C under nitrogen, which causes covalent bonding at the interface. Finally, the top silicon and SiGe layers are removed by chemical etching (e).

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